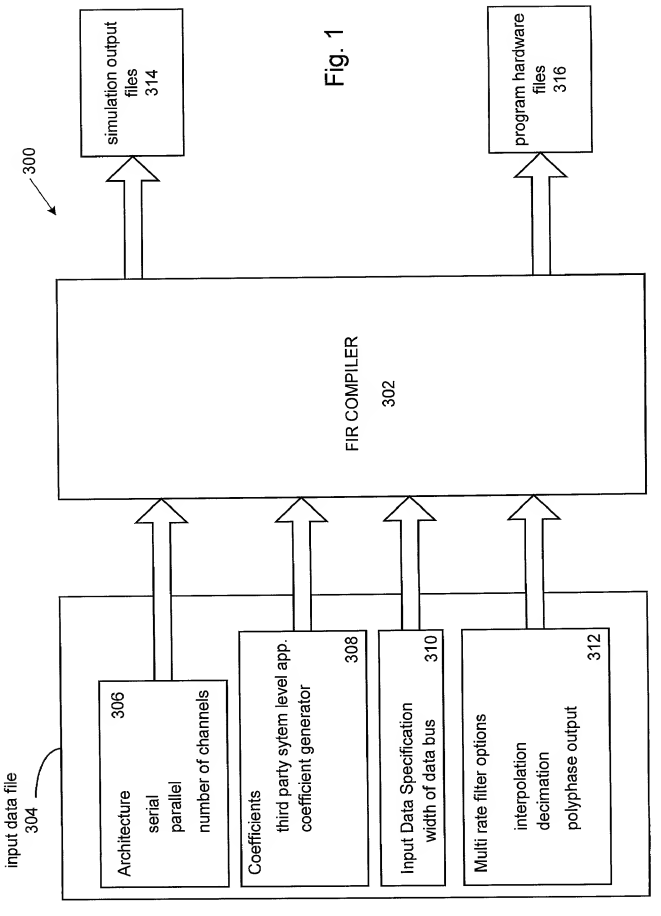

300
input data file
304
Architecture
306
serial
parallel
number of channels
Coefficients
third party sytem level app.
coefficient generator
308
Input Data Specification
width of data bus
310
Multi rate filter options
interpolation
decimation
polyphase output
312
FIR COMPILER
302
simulation output
files
314
program hardware
files
316

Fig. 1

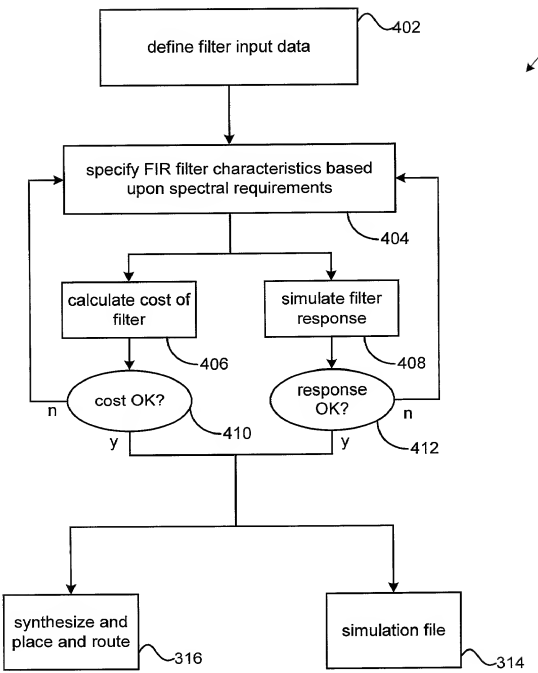

400
define filter input data
402
specify FIR filter characteristics based upon spectral requirements
404
calculate cost of filter
406
simulate filter response
408
cost OK?
410
response OK?
412
n
y
n
y
synthesize and place and route
316
simulation file
314

Fig. 2

Express Mail # EL580402171US
Filed: Herewith
Title: FINITE IMPULSE RESPONSE (FIR) FILTER COMPILER
Inventor: San et al.
Atty Docket No: ALTRP054
Page 3 of 16

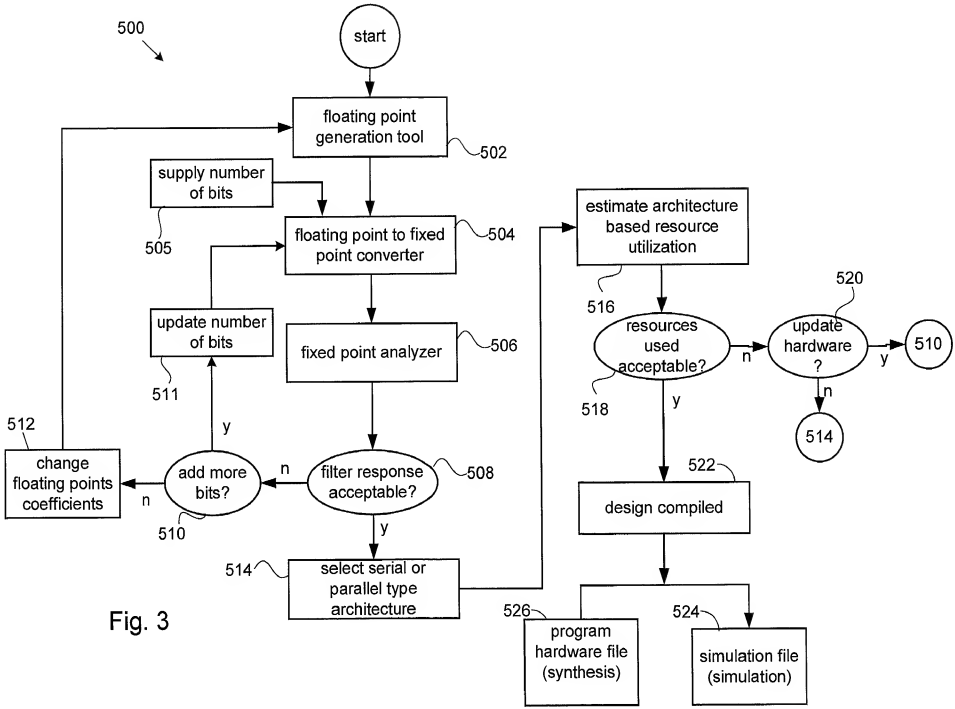


Fig. 3

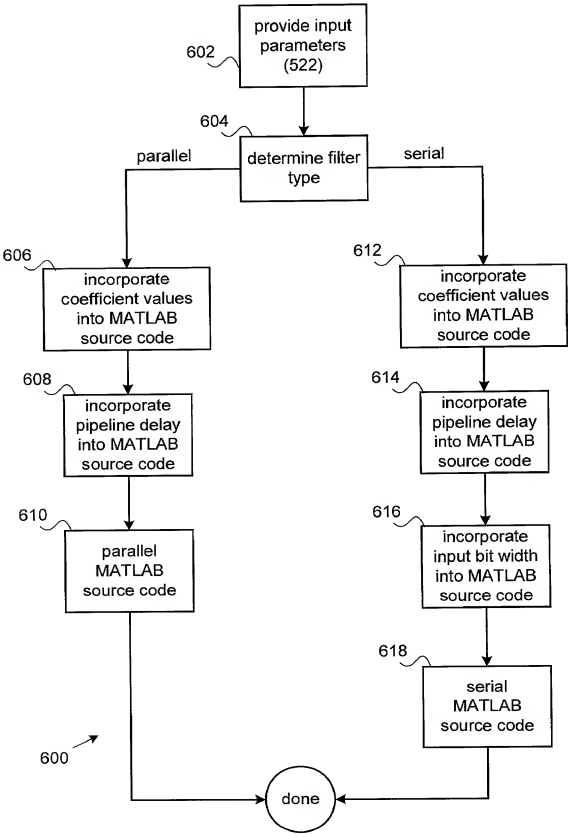
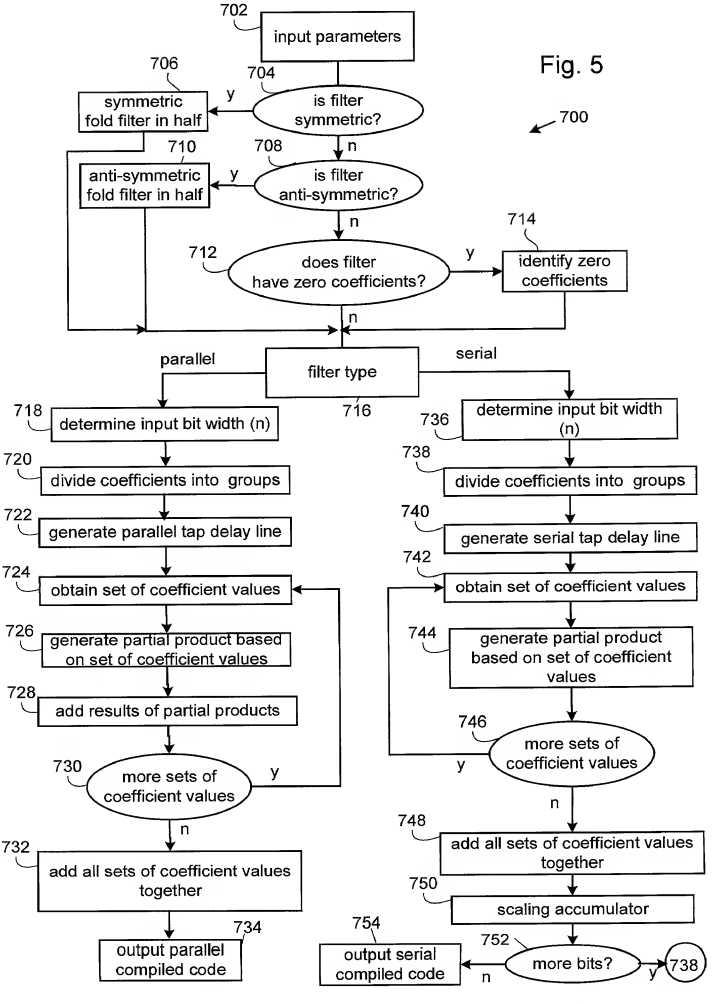

provide input parameters (522)
602
604
determine filter type
parallel
serial
606
incorporate coefficient values into MATLAB source code
608
incorporate pipeline delay into MATLAB source code
610
parallel MATLAB source code
612
incorporate coefficient values into MATLAB source code
614
incorporate pipeline delay into MATLAB source code
616
incorporate input bit width into MATLAB source code
618
serial MATLAB source code
600
done

Fig. 4

Fig. 5


700
702
input parameters
704
is filter symmetric?
y
706
symmetric fold filter in half
n
708
is filter anti-symmetric?
y
710
anti-symmetric fold filter in half
n
712
does filter have zero coefficients?
y
714
identify zero coefficients
n
filter type
716
parallel
serial
718
determine input bit width (n)
720
divide coefficients into groups
722
generate parallel tap delay line
724
obtain set of coefficient values
726
generate partial product based on set of coefficient values
728
add results of partial products
730
more sets of coefficient values
y
n
732
add all sets of coefficient values together
734
output parallel compiled code
736
determine input bit width (n)
738
divide coefficients into groups
740
generate serial tap delay line
742
obtain set of coefficient values
744
generate partial product based on set of coefficient values
746
more sets of coefficient values
y
n
748
add all sets of coefficient values together
750
scaling accumulator
752
more bits?
y
738
n
754
output serial compiled code

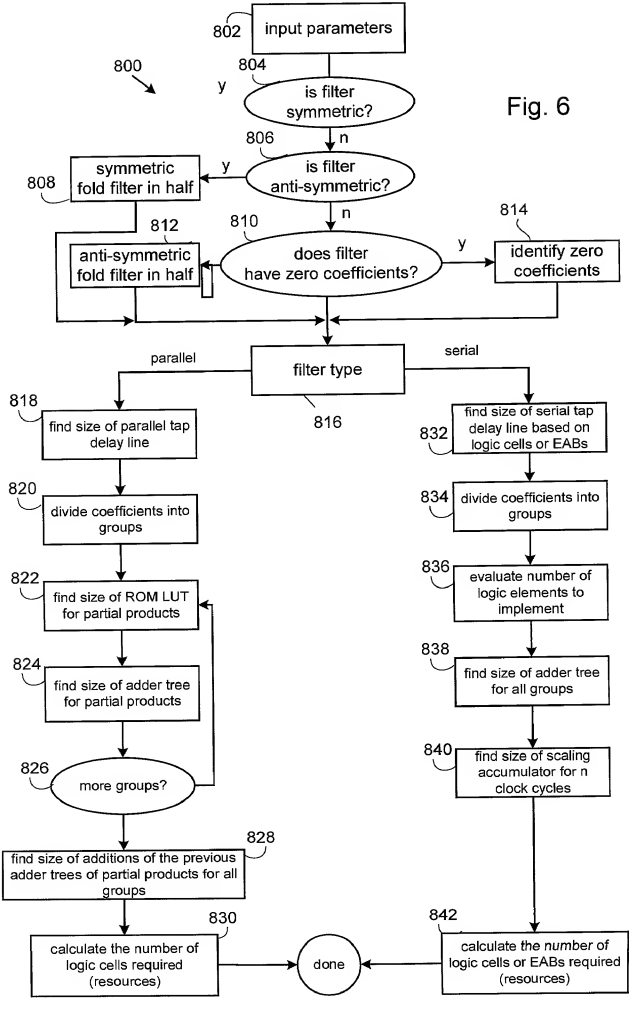
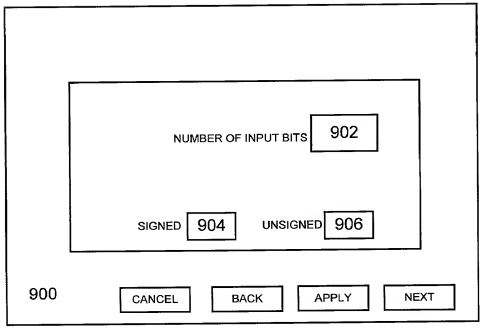
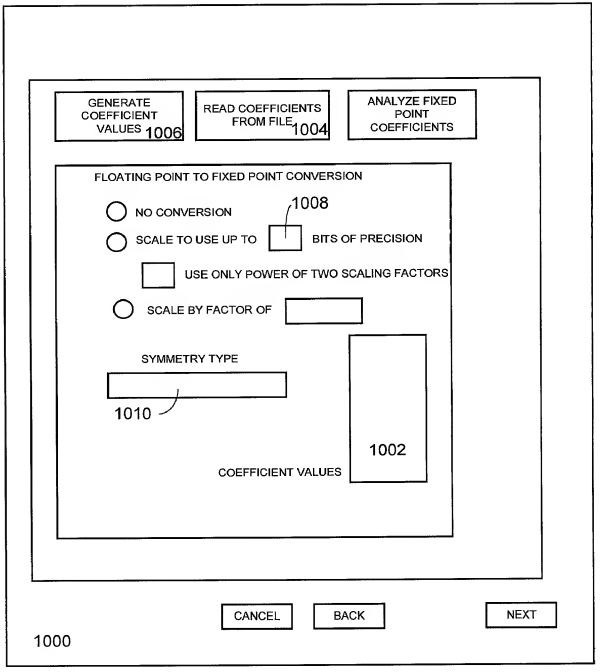

800
802
input parameters
804
is filter symmetric?
y
n
806
is filter anti-symmetric?
y
n
808
symmetric fold filter in half
810
does filter have zero coefficients?
y
812
anti-symmetric fold filter in half
814
identify zero coefficients
filter type
816
parallel
serial
818
find size of parallel tap delay line
820
divide coefficients into groups
822
find size of ROM LUT for partial products
824
find size of adder tree for partial products
826
more groups?
828
find size of additions of the previous adder trees of partial products for all groups
830
calculate the number of logic cells required (resources)
done
832
find size of serial tap delay line based on logic cells or EABs
834
divide coefficients into groups
836
evaluate number of logic elements to implement
838
find size of adder tree for all groups
840
find size of scaling accumulator for n clock cycles
842
calculate the number of logic cells or EABs required (resources)

Fig. 6



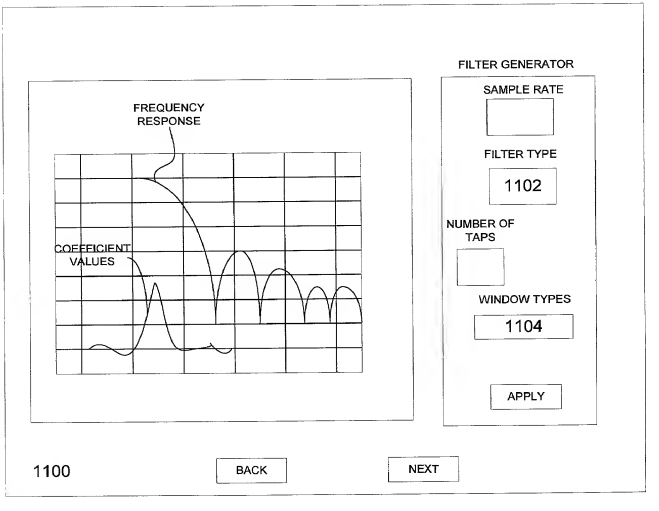
INPUT DATA BUS PARAMETERS

Fig. 7



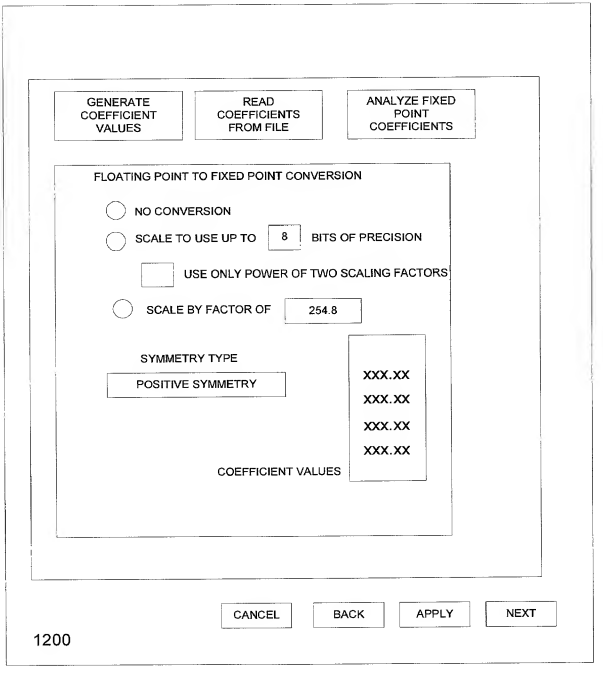
SPECIFY COEFFICIENTS

Fig. 8



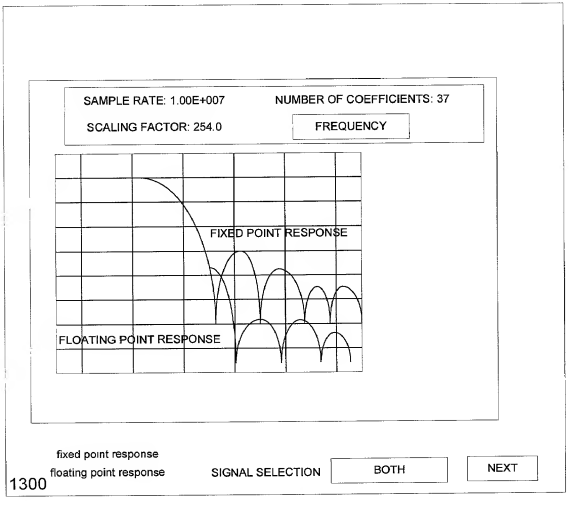
SCALED AND ROUNDED COEFFICIENTS

Fig. 9



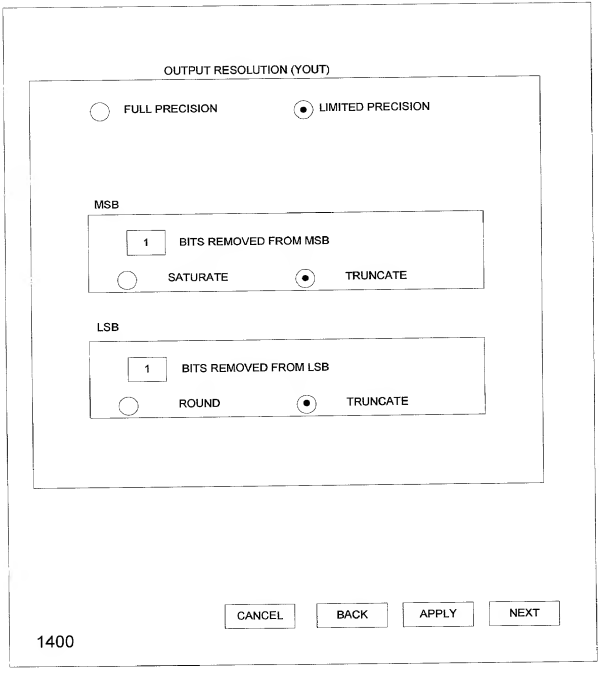
SPECIFY COEFFICIENTS

Fig. 10



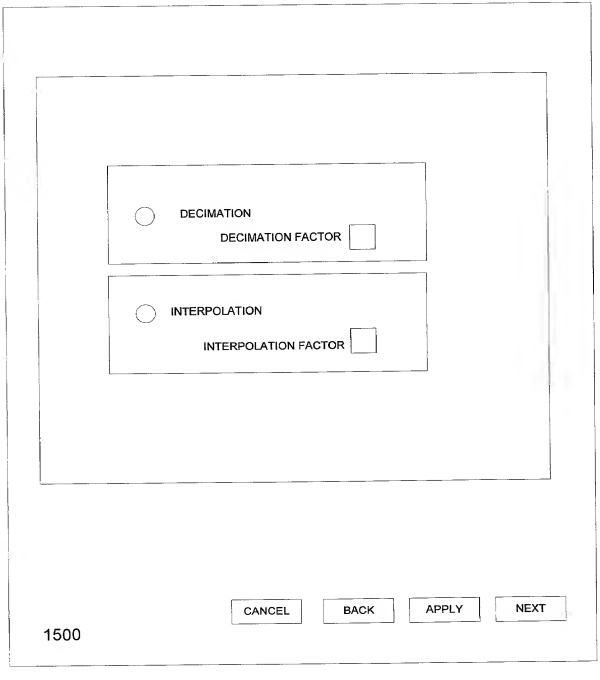
FIXED POINT COEFFICIENT ANALYZER

Fig. 11



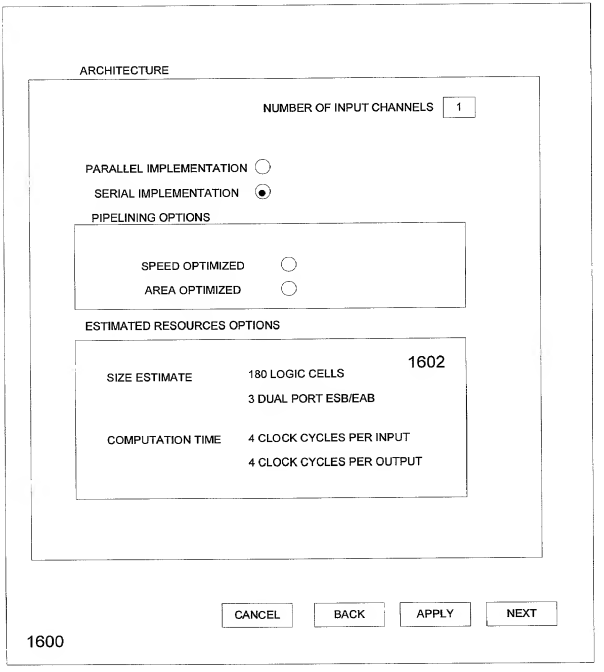
SPECIFY FILTER PRECISION

Fig. 12



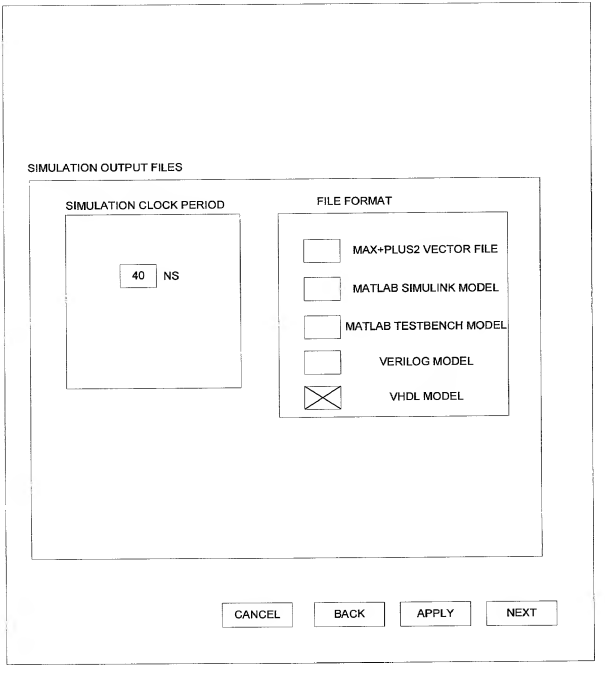
SPECIFY DECIMATION OR INTERPOLATION

Fig. 13



SPECIFY FILTER ARCHITECTURE

Fig. 14



CHOOSE OUTPUT FILE TYPES

Fig. 15

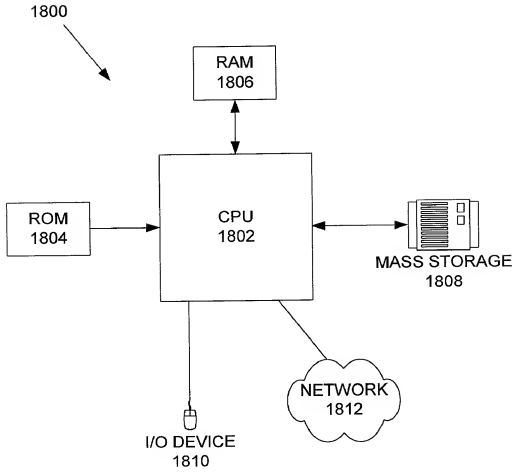

1800
RAM
1806
ROM
1804
CPU
1802
MASS STORAGE
1808
NETWORK
1812
I/O DEVICE
1810

Fig. 16